

Notice of Allowability

Application No.

09/398,707

Examiner

Mujtaba K Chaudry

Applicant(s)

POLK ET AL.

Art Unit

2133

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to 11/04/2004.
2. ☒ The allowed claim(s) is/are 13-26.
3. ☒ The drawings filed on 20 September 1999 are accepted by the Examiner.
4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 - a) ☐ All b) ☐ Some* c) ☐ None of the:
 1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

* Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.
 6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
 - (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
 - 1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
 - (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.
- Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

- | | |
|---|---|
| 1. <input type="checkbox"/> Notice of References Cited (PTO-892) | 5. <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 2. <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 6. <input type="checkbox"/> Interview Summary (PTO-413),
Paper No./Mail Date _____ |
| 3. <input type="checkbox"/> Information Disclosure Statements (PTO-1449 or PTO/SB/08),
Paper No./Mail Date _____ | 7. <input type="checkbox"/> Examiner's Amendment/Comment |
| 4. <input type="checkbox"/> Examiner's Comment Regarding Requirement for Deposit
of Biological Material | 8. <input checked="" type="checkbox"/> Examiner's Statement of Reasons for Allowance |
| | 9. <input type="checkbox"/> Other _____ |

REASONS FOR ALLOWANCE

Claims 13-26 are allowed. The following is an Examiner's statement of reasons for allowance:

Independent claim 13 of the present application teaches a modem apparatus comprising: an analog interface for interfacing to a communication line; a digital signal processor coupled to the analog interface, the digital signal processor being coupled perform frequency domain equalization (FEQ) operations, time domain equalization (TEQ) operations, fast Fourier transform (FFT) operations, inverse fast Fourier transform (iFFT) operations, and encoding/decoding operations on a serial stream of data provided through the analog interface, the digital signal processor having an output; a data bus coupled to the output of the digital signal processor; and a host central processing unit (CPU) coupled to the data bus for receiving packets of data from the digital signal processor, the host CPU performing error correction operations on the data within the packets of data, wherein at least one operation performed by one of the digital signal processor and the host CPU can be dynamically reassigned to a different one of the digital signal processor and the host CPU. The foregoing limitations are not found in the prior arts of record. The prior art of record, namely Modlin et al., teaches (title and abstract) a method and apparatus that provides flexibility in setting user data rates and managing delays in data transmission systems using a super-frame structure and Time Division Duplexing (TDD). Modlin teaches insertion of dummy words into a data stream to be transmitted. By inserting the dummy words, the apparatus is able to render codewords, symbols and super-frames independent from user data rates. As a result, a wide range of user data rates are available in data transmission systems using a super-frame and TDD. Modlin teaches (col. 3, lines 2-33 & figure 1B) a remote

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receiver 150 which receives analog signals that have been transmitted over a channel by a transmitter. The received analog signals are supplied to an analog-to-digital converter (ADC) 152, which converts the received analog signals to digital signals. The digital signals are then supplied to a Fast Fourier Transform (FFT) unit 154 that demodulates the digital signals while converting the digital signals from a time domain to a frequency domain as stated in the present application. The demodulated digital signals are then supplied to a frequency domain equalizer (FEQ) unit 156, which performs equalization on the digital signals so the attenuation and phase are equalized over the various frequency tones. Then, a data symbol decoder 158 receives the equalized digital signals, which decodes the equalized digital signals to recover the data, or bits of data, transmitted on each of the frequency tones. In decoding the equalized digital signals, the data symbol decoder 158 needs access to the bit allocation information and the energy allocation information that were used to transmit the data. Hence, the data symbol decoder 158 is coupled to a received bit allocation table 162 and a received energy allocation table 160 which respectively stores the bit allocation information and the energy allocation information that were used to transmit the data. The data obtained from each of the frequency tones is then forwarded to the forward error correction (FEC) unit 164. The FEC unit 164 performs error correction on the data to produce corrected data. The corrected data is then stored in a buffer 166. None of the prior art of record teach nor fairly suggest all the limitations in the independent claim 1 of the present application. In particular, the limitations of "...encoding/decoding operations on a serial stream of data provided through the analog interface, the digital signal processor having an output; a data bus coupled to the output of the digital signal processor; and a host central processing unit (CPU) coupled to the data bus for receiving packets of data from the digital

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signal processor, the host CPU performing error correction operations on the data within the packets of data, wherein at least one operation performed by one of the digital signal processor and the host CPU can be dynamically reassigned to a different one of the digital signal processor and the host CPU..." are not taught nor fairly suggested in the prior arts of record.

Independent claim 20 recites similar limitations and therefore are allowed for similar reasons.

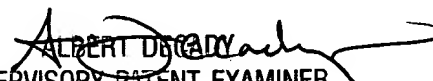
Dependent claims 14-19 and 21-26 depend from independent claims 13 and 20 and inherently include limitations therein and therefore are allowed as well.

Any inquiries concerning this communication should be directed to the examiner, Mujtaba Chaudry who may be reached at 571-272-3817. The examiner may normally be reached Mon – Thur 6:30 am to 4:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, please contact the examiner's supervisor, Albert DeCady at 571-272-3819.



Mujtaba Chaudry
Art Unit 2133
December 23, 2004



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